Parallel termination

By Hans Klos

Parallel termination is the simplest termination technique: A resistor, R_T, connects the open, or load, end of the transmission line to ground or V_{CC} (**Figure 1**).

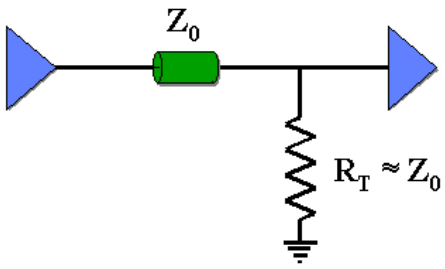

Figure 1. Parallel termination.

The value of R_T must match the characteristic impedance, Z_0 , of the line to eliminate reflections. If R_T matches Z_0, the termination resistor absorbs the energy that causes the reflection, regardless of the value of the termination voltage.

In digital logic, the sinking current is typically greater than the sourcing current. Terminating to V_{CC} helps the driver's sourcing capability, and terminating to ground helps its sinking capability. Hence, terminating to V_{CC} is better than terminating to ground, assuming a 50% duty cycle.

The advantages of parallel termination are that it offers simplicity of design and application and that it requires only one additional component, although you may ultimately use two resistors to terminate both ends of the line.

The disadvantages of this technique are that dc power dissipates in the termination resistor, which is typically 50 to 150V, and that constant dc current from the driver at high or low logic levels adds to the dc load of the driver. Also, parallel termination degrades the high-output level of the signal. Terminating TTL outputs to ground lowers the V_{OH} level, which reduces the noise immunity at the receiver input.

Parallel termination also results in a lower signal slew rate with a capacitive load than does an unterminated line. The load capacitance and the resistance (parallel combination of termination resistance and Z_0) add to the RC time constant of the signal, which rises to the driver's output voltage. Note that the voltage at the end of an unterminated line doubles and hence produces a faster slew rate.

The effect of different termination techniques on the slew rate of the signal at the end of the line is the outcome of complex interactions between the transmission line and the RC delay involved. When you use parallel termination, you should be aware that a line impedance of less than 100V terminated with this scheme requires a dc output of 24 mA for TTL levels (V_{OH}(MIN) =2.4V).
For this reason, parallel termination is not recommended for a battery-driven system. Also, note that the termination resistor dissipates as much as 0.25W (50 mA through a 100V resistor) of power, which a CMOS system that consumes only a few milliwatts of power can't accom-modate. Also, remember that the power dissipation depends on the duty cycle: Connecting the resistor to ground results in the lowest power dissipation for low duty cycles, and ter-minating to V_{CC} results in the lowest power dissipation for high duty cycles. In addition, a strong pull-down resistor might cause the falling edge to be faster than the rising edge, resulting in the distortion of the duty cycle of the signal.

(Reference: Termination techniques for high speed buses by Karthik Ethirajan and John Nemec)