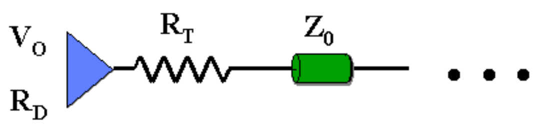
Series termination

By Hans Klos

Series termination, also called back-matching, is a source-end termination. A series termination comprises a resistor between the driver's output and the transmission line (**Figure 1**).



$$R_D + R_T \approx Z_0$$

Figure 1. Series termination.

The valueof the series resistor plus the output impedance of the driving gate should equal Z_0 (characteristic impedance of the transmission line).

With this type of termination, only one-half the signal value appears on the line because of the voltage division between the line and the combination of the series resistor and the driver's impedance.
At the receiving end, however, the mismatch between the line impedance and the receiver's typically high input impedance causes a reflection of approximately the same voltage magnitude as the incident signal. The receiving device immediately sees the full voltage (the sum of the incident and reflected voltages), and the added signal propagates to the driving end. However, no further reflections occur because the series resistor terminates the reflected wave at the driving end.

The advantages of series termination are that it adds only one resistor per driver for the system and that its termination resistor consumes less power than all the other resistive types of termination. Series termination also adds no dc load to the driver and offers no extra impedance from signal line to ground.

The disadvantages of series termination are that using this method makes it difficult to tune the value of the series resistance so that the received-signal amplitude (after the first reflection) falls within the switching threshold and noise budget.

Also, most drivers are nonlinear; the output impedance varies with the logic state of the device. This makes it difficult to tune the optimum series resistor value. It is also difficult to select a good value for the series resistance by applying a simple design equation.

Another disadvantage of series termination is that the driving end of the transmission line does not see the full reinforced signal amplitude for as long as twice the propagation delay of the line. The diminished signal amplitude during this time reduces some of the receiver's noise immunity in a multidrop situation. Also, with series termination, the data setup time for digital signals of the receiver (part of its timing budget) must accommodate this propagation delay.

Series termination also results in a lower signal slew rate with a capacitive load than does parallel termination. The load capacitance and the Z_0 of the line add to the RC time constant of the signal, which rises to one-half the driver's output voltage.

The applications for series termination include CMOS-to-CMOS connections because series termination adds no impedance from signal line to ground. This termination also works well for advanced CMOS logic families, such as FACT and ECL. With FACT devices, the series termination resistor adds to the output impedance of the driver. Thus, the driver

dissipates less power than it does without the termination.
Series termination also works well for systems with loads lumped at the end of the cable as opposed to a multidrop situation. In a multidrop situation, receivers on the line see the full amplitude of the signal at different times. You can eliminate the disadvantages of higher propagation delay and usage with lumped loads only by using more transmission lines. If the driver has high fan-out, then you can connect many transmission lines N, for example to the driver's output. Each line then needs its own series termination according to the design equation.
The net impedance at the output of the driver is $(R+Z_0)/N$. This net impedance must be much larger than the internal impedance of the driver for the driver itself to function.

(Reference: Termination techniques for high speed buses by Karthik Ethirajan and John Nemec)

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