Thevenin termination

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Thevenin termination is becomming very important in modern digital systems. Thevenin termination uses two resistors, R_{TH} and R_{TL} (Figure 1.), whose parallel combination matches the characteristic impedance (Z_0) of the transmission line.

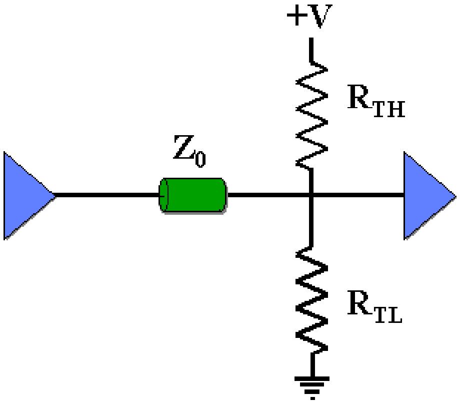

Figure 1. *Thevenin termination*

The Thevenin voltage, $V_{TH} = V_{TL}$, must be such that the driver's I_{OH} and I_{OL} currents are within the driver's specifications. Resistor R_{TH} helps the driver to easily pull up to a logic-high state by sourcing some current to the load. Similarly, Resistor R_{TL} helps the driver to pull down to a logic-low state by sinking some current to ground.

Well chosen values for R_{TH} and R_{TL} enhance the driver's fan-out and smooth the power dissipation variations because of the change in duty cycles. The advantages of Thevenin termination are that the termination resistors also serve as pull-up and pull-down resistors and thereby improve the noise margin of the system. Thevenin termination also reduces the burden on the driver by supplying additional current to the load. This additional current helps the driver especially in a large voltage-swing system, such as 5 and 3.3V CMOS- or Bi-CMOS- based systems. Also, this type of termination provides good overshoot suppression.

One disadvantage of Thevenin termination is that a constant flow of dc from V_{CC} to ground, regardless of the logic state, results in static power dissipation in the termination resistors. This method also requires ratio resistors and additional power and ground connections. Also, a line voltage, which equals the Thevenin voltage on a tri-stated bus, close to the switching threshold voltage causes greater levels of power dissipation within CMOS logic devices. At a voltage close to the threshold, both NMOS and PMOS transistors are conducting, which results in a current path between V_{CC} and ground.

Thevenin termination also results in a lower signal slew rate with a capacitive load than does an unterminated line. The load capacitance and the resistance (parallel combination of Z_0, R_{TH} and R_{TL}) add to the RC time constant of the signal, which rises to the driver's output voltage. Note that CMOS devices switch at 50% threshold. Hence, when using Thevenin termination for CMOS devices, equal values for R_{TH} and R_{TL} result in a line voltage of one-half the V_{CC}. This situation occurs when a logic device does not drive the line. The result is greater levels of power dissipation with-in the receiver. The sum of this dissipation and the power dissipation in the termination resistors may be unacceptably high for CMOS logic devices.

In this arrangement, the parallel combination of R_{TH} and R_{TL} must equal Z_0. The ratio R_{TH}/R_{TL} controls the relative proportions of HI and LO drive current. The selection of values for R_{TH} and R_{TL} is best done graphically. The selection is controlled by three constraints:

1) The parallel combination of R_{TH} and R_{TL} must equal Z_0
2) We must not exceed I_{OHmax} (maximum high-level output current)
3) We must not exceed I_{OLmax} (maximum low-level output current)

Current entering the driver (sink current) is positive, while current leaving the driver (source current) is negative.

1) The first constraint is easily expressed in the admittance domain.

$$Y_1 = 1/R_{TH} \text{ and } Y_2 = 1/R_{TL}$$

The first constraint looks like this:

$$Y_1+Y_2=1/Zo$$

It appears as a diagonal line on the constraint graph. A valid combinations of Y_1 and Y_2 lie on this line.

2) Derive an equation for the second constraint by noting that the current into the driver equals the current flowing in R_2 minus the current flowing in R_1. These two currents depend on voltages Vcc, Vee and the driver output voltage. See constraint:

$$(V_{CC}-V_{OH})Y_1 - (V_{OH}-V_{EE})Y_2 > I_{OHmax}$$

3) The same constraint can be made for the LO state:

$$(V_{CC}-V_{OL})Y_1 - (V_{OL}-V_{EE})Y_2 < I_{Olmax}$$

The following information is derived from a datasheet.

$V_{OH} = 2.4V$, $I_{OH} = -16mA$
$V_{OL} = 0.45V$, $I_{OL} = 46mA$

Other settings:
$V_{CC} = 3.3V$, $V_{EE} = 0V$
$Z_O = 50\ \Omega$

With this information, the three constraints are:

1) $Y_1+Y_2 = 0.02$
2) $0.9Y_1 - 2.4Y_2 > -0.016$
3) $2.85Y_1 - 0.45Y_2 > 0.046$

The constraints are displayed in figure 2.

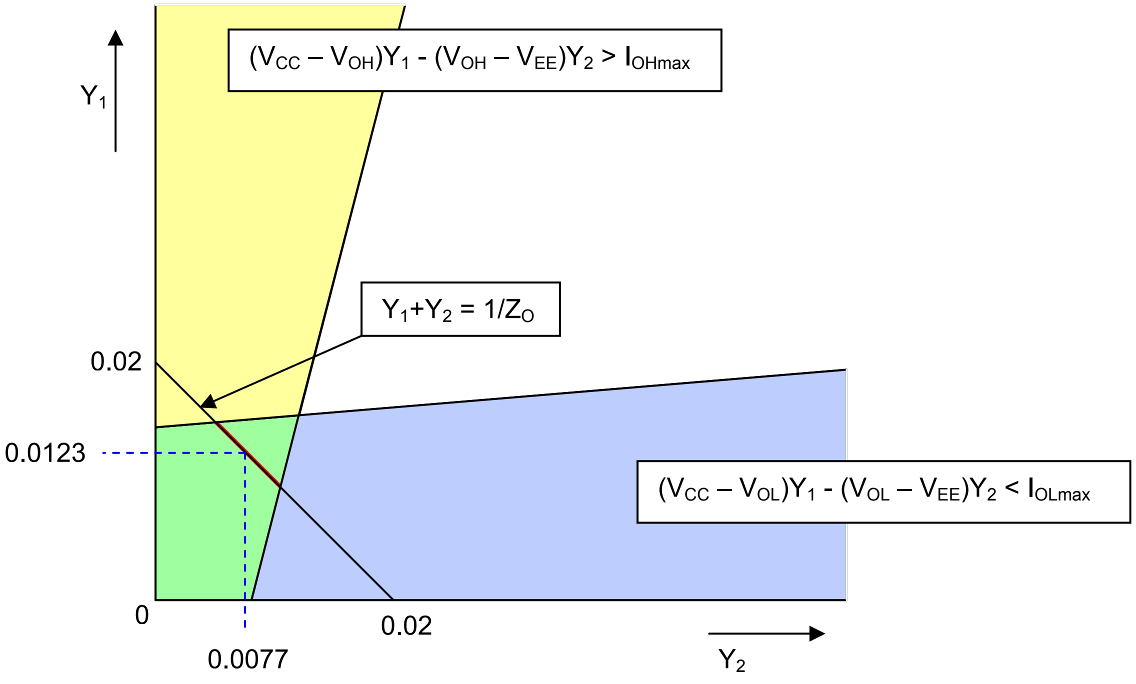

***Figure 2.** Thevenin termination constraints.*

Explanation:

🟨 = Region satisfying output high current requirements.

🟦 = Region satisfying output low current requirements.

🟩 = Region satisfying both current constraints.

— = Impedance constraint line within the green region (Y_1 and .Y_2 should lie on this line).

- - - = Example of Y_1 and Y_2 admittance values.

(Reference: Termination techniques for high speed buses by Karthik Ethirajan and John Nemec)